A Chronology of Major Events in Parallel Computing

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Abstract

This report is a point-form chronology of major developments in parallel computing and supercomputing from the 1950s to 1992. The emphasis is on commercial systems; theoretical ideas and academic research projects are included only where the author knows them to have had a significant influence on users.

1 Introduction

This document is a chronology of major developments in parallel computing and supercomputing. In order to keep its size manageable, I have emphasized commercial systems; theoretical ideas and academic research projects have been included only where I knew that they had influenced vendors and users. Information more recent than the end of 1992 has deliberately been left out, as the author felt that it would be impossible to judge the importance (or otherwise) of more recent events.

Many people have contributed or corrected articles over the past year, mostly through the Internet newsgroups `comp.parallel` and `comp.sys.super`. I am particularly grateful to Michael Wolfe, without whose early contributions this project would not have happened, and to Eugene Miya, who provided pointers and advice. I am also grateful to Andy Ben-Dyke, Graem Ringwood, and Paul Whiting for material on functional, logic and dataflow programming respectively, and to Richard Walker, who helped with the layout and printing of the poster form of this document. A wall-chart version of this document is also available in FrameMaker format, but requires a printer capable of producing a 36″×200″ page.

2 Events

1955

1 : IBM introduces the 704. Principal architect is Gene Amdahl; it is the first commercial machine with floating-point hardware, and is capable of approximately 5 kFLOPS. (PG: IBM 704; Amdahl,

Gene)

1956

2 : IBM starts 7030 project (known as STRETCH) to produce supercomputer for Los Alamos National Laboratory (LANL). Its goal is to produce a machine with 100 times the performance of any available at the time. (WM, KHG, SMK: IBM STRETCH; LANL; AEC)

3 : LARC (Livermore Automatic Research Computer) project begins to design supercomputer for Lawrence Livermore National Laboratory (LLNL). (WM, KHG, SMK: LANL; Remington Rand; LARC; AEC)

4 : Atlas project begins in the U.K. as joint venture between University of Manchester and Ferranti Ltd. Principal architect is Tom Kilburn. (IRN: Atlas; University of Manchester; Kilburn, Tom; Ferranti)

1957

5 : Digital Equipment Corporation (DEC) founded. (WGV: DEC)

1958

6 : Control Data Corporation (CDC) founded. (LNR: CDC)

7 : Bull of France announces the Gamma 60 with multiple functional units and fork & join operations in its instruction set. 19 are later built. (SMK: Bull Gamma 60)

8 : John Cocke and Daniel Slotnick discuss use of parallelism in numerical calculations in an IBM research memo. Slotnick later proposes SOLOMON, a SIMD machine with 1024 1-bit PEs, each with memory for 128 32-bit values. The machine is never built, but the design is the starting point for much later work. (GFAW, KHG: SOLOMON; Slotnick, Daniel; Cocke, John)

1959

9 : IBM delivers first STRETCH computer. A total of eight are built; much of the technology is re-used in the IBM 7090 which is delivered this same year. (WM, KHG, CJ: IBM STRETCH)

10 : First LARC delivered; although it meets its performance specifications, only two are ever built. (SMK, KHG: Remington Rand; LARC)

1960

11 : Control Data starts development of CDC 6600. (WM: Cray, Seymour; CDC 6600)

12 : Honeywell introduces Honeywell 800, with hardware support for timesharing between eight programs. (SM: Honeywell 800)

13 : E. V. Yevreinov at the Institute of Mathematics in Novosibirsk (IMN) begins work on tightly-coupled, coarse-grain parallel architectures with programmable interconnects. (WcP: Yevreinov, E. V.; IMN)

1961

1962

14 : CDC delivers first CDC 1604. Machine is similar to IBM 7090, featuring 48 bit words and a 6 μsec memory cycle time. (MEN, LNR: CDC 1604; Cray, Seymour; Thornton, Jim)

15 : Atlas computer becomes operational. It is the first machine to use virtual memory and paging; its instruction execution is pipelined, and it contains separate fixed- and floating-point arithmetic units, capable of approximately 200 kFLOPS. (IRN: Atlas; Ferranti; University of Manchester)

16 : C. A. Petri describes Petri Nets, a theoretical framework for describing and analyzing the properties of concurrent systems. (HW: Petri, C. A.; Petri Nets)

17 : Burroughs introduces the D825 symmetrical MIMD multiprocessor. 1 to 4 CPUs access 1 to 16 memory modules using a crossbar switch. The CPUs are similar to the later B5000; the operating system is symmetrical, with a shared ready queue. (JDW: Burroughs D825)

1963

1964

18 : Control Data Corporation produces the CDC 6600, the first supercomputer to be both a technical and commercial success. Each machine contained one 60-bit CPU and 10 peripheral processing units (PPUs); the CPU used a scoreboard to manage instruction dependencies. (WGV, MD, BL: CDC 6600; Cray, Seymour; Thornton, Jim)

19 : IBM begins design of the Advanced Computer System (ACS), capable of issuing up to seven instructions per cycle. The project was shelved in 1969, but many of the techniques were incorporated into later IBM machines. (SMK: IBM; superscalar; ACS; Cocke, John)

20 : Daniel Slotnick proposes building a massively-parallel machine for the Lawrence Livermore National Laboratory (LLNL); the Atomic Energy Commission gives the contract to CDC instead, who build the STAR-100 to fulfil it. Slotnick's design funded by the Air Force, and evolves into the ILLIAC-IV. The machine is built at the University of Illinois, with Burroughs and Texas Instruments as primary subcontractors. Texas Instruments' Advanced Scientific Computer (ASC) also grows out of this initiative. (WM, MD: Slotnick, Daniel; AEC; ILLIAC-IV; CDC STAR-100; TI ASC; LLNL)

1965

21 : GE, MIT, and AT&T Bell Laboratories start work on Multics. The project's aim is to develop a general-purpose shared-memory multiprocessing timesharing system. (MB: GE; MIT; Bell Labs; Multics; multiprocessor, symmetric)

22 : Edsger Dijkstra describes and names the critical regions problem. Much later work in concurrent systems is devoted to finding safe, efficient ways to manage critical regions. (AnG: Dijkstra, Edsger; critical regions)

23 : James W. Cooley and John W. Tukey describe the Fast Fourier Transform algorithm, which is later one of the largest single consumers of floating-point cycles. (MEN: FFT; Cooley, James W.; Tukey, John W.)

1966

24 : Arthur Bernstein introduces Bernstein's Condition for statement independence (the foundation of subsequent work on data dependence analysis). (WGV: Bernstein, Arthur; data dependence)

25 : CDC introduces CDC 6500, containing two CDC 6400 processors. Principal architect is Jim Thornton. (LNR, BWE: CDC 6500; Thornton, Jim)

26 : The UNIVAC division of Sperry Rand Corporation delivers the first multiprocessor 1108. Each contains up to 3 CPUs and 2 I/O controllers; its EXEC 8 operating system provides interface for multithread program execution. (FRM, GMD: UNIVAC 1108; multiprocessor)

27 : Michael Flynn publishes a paper describing the architectural taxonomy which bears his name. (WGV: Flynn, Michael; taxonomy)

28 : The Minsk-222 completed by E. V. Yevreinov at the Institute of Mathematics, Novosibirsk. (WcP: Yevreinov, E. V.; Minsk-222; IMN)

1967

29 : Karp, Miller and Winograd publish paper describing the use of dependence vectors and loop transformations to analyze data dependencies. (WM: vectorization; program transformation)

30 : IBM produces the 360/91 (later model 95) with dynamic instruction reordering. 20 of these are produced over the next several years; the line is eventually supplanted by the slower Model 85. (WM, KHG: IBM 360/91)

31 : BESM-6, developed at Institute of Precision Mechanics and Computer Technology (ITMVT) in Moscow, goes into production. Machine has 48-bit words, achieves 1 MIPS, and contains virtual memory and a pipelined processor. (WcP: BESM-6; ITMVT)

32 : Gene Amdahl and Daniel Slotnick have published debate at AFIPS Conference about the feasibility of parallel processing. Amdahl's argument about limits to parallelism becomes known as "Amdahl's Law"; he also propounds a corollary about system balance (sometimes called "Amdahl's Other Law"), which states that a balanced machine has the same number of MIPS, Mbytes, and Mbit/s of I/O bandwidth. (MEN, WGV: Amdahl, Gene; Slotnick, Daniel; Amdahl's Law)

1968

33 : Duane Adams of Stanford University coins the term "dataflow" while describing graphical models of computation in his Ph.D thesis. (WPG: dataflow; Stanford University; Adams, Duane)

34 : Group formed at Control Data to study the computing needs of image processing; this leads to the CDC AFP and Cyberplus designs. (WM: CDC Cyberplus; CDC AFP)

35 : IBM 2938 Array Processor delivered to Western Geophysical (who promptly paint racing stripes on it). First commercial machine to sustain 10 MFLOPS on 32-bit floating-point operations. A programmable digital signal processor, it proves very popular in the petroleum industry. (KHG, PG: IBM 2938; array processor)

36 : Edsger Dijkstra describes semaphores, and introduces the dining philosophers problem, which later becomes a standard example in concurrency theory. (WGV, HW, AnG: Dijkstra, Edsger; semaphore; dining philosophers)

1969

37 : George Paul, M. Wayne Wilson, and Charles Cree begin work at IBM on VECTRAN, an extension to FORTRAN 66 with array-valued operators, functions, and I/O facilities. (PG, BL: IBM; FORTRAN; VECTRAN; data parallelism; programming languages)

38 : CDC produces the CDC 7600 pipelined supercomputer as a follow-on to the CDC 6600. (WGV: Cray, Seymour; CDC 7600)

39 : Work begins at Compass Inc. on a parallelizing FORTRAN compiler for the ILLIAC-IV called IVTRAN. (PDL: Compass; parallelization; ILLIAC-IV)

40 : Honeywell delivers first Multics system (symmetric multiprocessor with up to 8 processors). (MB: Honeywell; Multics; multiprocessor, symmetric)

1970

41 : Floating Point Systems Inc. founded by C. N. Winningstad and other former Tektronix employees. The company's mission is to manufacture floating-point coprocessors for minicomputers. (WGV, CBR: FPS)

42 : PDP-6/KA10 asymmetric multiprocessor jointly developed by MIT and DEC. (FJM: DEC; multiprocessor, asymmetric; MIT)

43 : Work on El'brus multiprocessors begins at ITMVT under direction of Vsevolod S. Burtsev. Each machine contains up to 10 CPUs, with shared memory and hardware support for fault tolerance. (WcP: El'brus-1; ITMVT; Burtsev, Vsevolod S.)

44 : Development of C.mmp multiprocessor begins at Carnegie-Mellon with support from DEC. (WGV: C.mmp; CMU)

1971

45 : CDC delivers hardwired Cyberplus parallel radar image processing system to Rome Air Development Center, where it achieves 250 times the performance of a CDC 6600. (WM: CDC Cyberplus)

46 : Intel produces the world's first single-chip CPU, the 4004 microprocessor. (WGV: Intel)

47 : Texas Instruments delivers the first Advanced Scientific Computer (also called Advanced Seismic Computer), containing 4 pipelines with an 80 ns clock time. Vector instructions were memory-to-memory. Seven of these machines are later built, and an aggressive automatic vectorizing FORTRAN compiler is developed for them. It is the first machine to contain SECDED (Single Error Correction, Double Error Detection) memory. (WM, AnP: TI ASC; vectorization)

1972

48 : Seymour Cray leaves Control Data Corporation to found Cray Research Inc. CDC cancels the 8600 project, a follow-on to the 7600. (WGV: CRI; Cray, Seymour)

49 : DEC rewrites the TOPS-10 monitor software for the PDP-10 to allow asymmetric multiprocessing. (FJM, RP: DEC; multiprocessor, asymmetric)

50 : Quarter-sized (64 PEs) ILLIAC-IV installed at NASA Ames. Each processor has a peak speed of 4 MFLOPS; the machine's I/O system is capable of 500 Mbit/s. (WGV: ILLIAC-IV; NASA Ames)

51 : Paper studies of massive bit-level parallelism done by Stewart Reddaway at ICL. These later lead to development of ICL DAP. (WGV: ICL; ICL/AMT DAP; Reddaway, Stewart)

52 : BBN builds first Pluribus machines as ARPAnet switch nodes. The switching technology developed for this project later reappears in BBN's Butterfly multiprocessors. (WGV: BBN Pluribus)

53 : Harold Stone describes the perfect shuffle network, a multi-stage interconnection network which is the basis for much later work on parallel computer topologies. (WGV: Stone, Harold; perfect shuffle network)

54 : Tony Hoare and Per Brinch Hansen independently introduce the concept of conditional critical regions, which later influences languages such as Ada and SR. (AnG: conditional critical regions; Hoare, Tony; Brinch Hansen, Per)

55 : Goodyear produces the STARAN, a 4×256 1-bit PE array processor using associative addressing and a FLIP network. (SMC: Goodyear STARAN)

56 : Burroughs begins building the PEPE (Parallel Element Processor Ensemble) which contains 8×36 processing elements and uses associative addressing. (SMC: Burroughs PEPE)

1973

57 : William L. Cohagan, working for Texas Instruments on a compiler for the TI ASC, describes the GCD test for data dependence analysis. (WM: TI ASC; vectorization; GCD test; Cohagan, William)

58 : Thacker, Lampson, Boggs, Metcalfe, and (many) others at the Xerox Palo Alto Research Center design and build the first Alto workstations and Ethernet local-area network. The potential of using clustered descendents of these machines as supercomputers widely acknowledged by early 1990s. (MEN: distributed computing; Xerox)

59 : Linear algebra community starts de facto standards activity. The resulting software is called the Basic Linear Algebra Subprograms (BLAS); its name is later changed to Level 1 BLAS. (DJ, DCJ: BLAS-1; standards)

1974

60 : Jack Dennis and David Misunas at MIT publish the first description of a dataflow computer. (WPG: MIT; dataflow)

61 : Leslie Lamport's paper "Parallel Execution of Do-Loops" lays the theoretical foundation for most later research on automatic vectorization and shared-memory parallelization. Much of the work was done in 1971-2 while Lamport was at Compass Inc. (ZH, PDL: Lamport, Leslie; vectorization; Compass)

62 : CDC delivers the STAR-100, the first commercial pipelined vector supercomputer, to the Lawrence Livermore National Laboratory. The machine uses a memory-to-memory architecture; its principal architects are Jim Thornton and Neil Lincoln. (LNR: CDC STAR-100; LLNL; Thornton, Jim; Lincoln, Neil)

63 : The Japanese National Aerospace Laboratory (NAL) and Fujitsu begin development of the first Japanese pipelined vector processor, the FACOM-230. Only two

of these machines are ever built. (HN: Fujitsu FACOM-230; NAL)

64 : IBM delivers the first 3838 array processor, a general-purpose digital signal processor. (KHG: IBM 3838; array processor)

65 : Work begins at Burroughs on designing the Burroughs Scientific Processor (BSP). (WM: Burroughs BSP)

66 : Work begins at ICL on building a prototype DAP (Distributed Array Processor). (WGV: ICL; ICL/AMT DAP)

67 : Burton Smith begins designing the context-flow Heterogeneous Element Processor (HEP) for Denelcor. (WGV: Denelcor HEP; Smith, Burton)

68 : Tony Hoare describes monitors, a structured mutual exclusion mechanism which is later incorporated into many concurrent programming languages. (WGV: Hoare, Tony; monitors)

69 : The LINPACK Project begins to develop software to solve linear systems of equations. (DJ, DCJ: LINPACK; standards)

70 : Tandem Computers founded by Jim Treybig and others from Hewlett-Packard to develop fault-tolerant systems for online transaction processing. (HB: Tandem; fault tolerance)

1975

71 : Cyber 200 project begins at Control Data; its architecture is to be memory-to-memory, like that of the STAR-100. Its principal architect is Neil Lincoln. (WM: CDC Cyber 200; Lincoln, Neil)

72 : ILLIAC-IV becomes operational at NASA Ames after concerted check-out effort. (WM: ILLIAC-IV; NASA Ames)

73 : Duncan Lawrie describes the Omega network, a multi-stage interconnection network which is later used in several parallel computers. (WGV: Lawrie, Duncan; Omega network)

74 : Work begins at Carnegie-Mellon University on the Cm* multiprocessor, with support from DEC. The machine combines PDP minicomputers using hierarchical buses. (WGV: CMU; Cm*; DEC)

75 : Edsger Dijkstra describes guarded commands, a mechanism for structuring concurrency which is later incorporated into many programming languages. (HW: Dijkstra, Edsger; guarded commands)

76 : Design of the iAPX 432 symmetric multiprocessor begins at Intel. (WGV: Intel iAPX 432)

1976

77 : The Parafrase compiler system is developed at University of Illinois under the direction of David Kuck. A successor to a program called the Analyzer, Parafrase is used as a testbed for the development of many new ideas on vectorization and program transformation. (WM: vectorization; Kuck, David; Parafrase; University of Illinois)

78 : Carl Hewitt, at MIT, invents the Actors model, in which control structures are patterns of messages. This model is the basis for much later work on high-level parallel programming models. (HP: Actors)

79 : Floating Point Systems Inc. delivers its first 38-bit AP-120B array processor. The machine issues multiple pipelined instructions every cycle. (CBR: FPS AP-120B; array processor; LIW)

80 : Cray Research delivers the first Freon-cooled CRAY-1 to Los Alamos National Laboratory. (WM, MEN: CRI CRAY-1; LANL; Cray, Seymour)

81 : Fujitsu delivers the first FACOM-230 vector processor to the Japanese National Aerospace Laboratory (NAL). (HN: Fujitsu FACOM-230; NAL)

82 : Tandem ships its first NonStop fault-tolerant disjoint-memory machines with 2 to 16 custom processors, dual interprocessor buses, and a message-based operating system. The machines are used primarily for on-line transaction processing. (HB: Tandem NonStop; fault tolerance)

83 : Work on the PS-2000 multiprocessor begins at the Institute of Control Problems in Moscow (IPU) and the Scientific Research Institute of Control Computers in Severodonetsk, Ukraine (NIIUVM). (WcP: PS-2000; IPU; NIIUVM)

84 : Utpal Banerjee's thesis at the University of Illinois formalizes the concept of data dependence, and describes and implements the analysis algorithm named after him. (WM, ZH: vectorization; Banerjee, Utpal; University of Illinois)

85 : CDC delivers the Flexible Processor, a programmable signal processing unit with a 48-bit instruction word. (WM, ND: CDC Flexible Processor)

86 : Borroughs delivers the PEPE associative processor. (SMC: Burroughs PEPE)

87 : Floating Point Systems Inc. describes loop wrapping (later called software pipelining), which it uses to program pipelined multiple instruction issue processors. (CBR: FPS; software pipelining; array processor)

1977

88 : Al Davis of the University of Utah, in collaboration with Burroughs, builds the DDM1, the first operational dataflow processor. (WPG: Davis, Al; University of Utah; Burroughs; DDM1; dataflow)

89 : Haendler, Hofmann, and Schneider built the Erlangen General Purpose Architecture (EGPA) machines at the University of Erlangen in Germany. Each machines contains 5 or 21 32-bit processors in a pyramid topology, and is programmed in an extension of FORTRAN 77. (SMC: EGPA; University of Erlangen)

90 : Roger Hockney introduces $n_{1/2}$ and r_∞ as metrics for pipeline performance. (HRW: performance metrics, $n_{1/2}$; performance metrics, r_∞; Hockney, Roger)

91 : C.mmp multiprocessor completed at Carnegie-Mellon University. The machine contains 16 PDP-11 minicomputers connected by a crossbar to shared memories, and supports much early work on languages and operating systems for parallel machines. (WGV: CMU; C.mmp)

92 : Conservative parallel discrete event simulation techniques are proposed independently by R. E. Bryant, and by K. Mani Chandy and J. Misra. (WGV: discrete event simulation; Chandy, K. Mani; Misra, J.; Bryant, R. E.)

93 : Massively Parallel Processor (MPP) project for fast image processing first discussed by Goodyear and NASA Goddard Space Flight Center. (WM, MEN: Goodyear MPP; NASA Goddard)

1978

94 : Arvind, Kim Gostelow and Wil Plouffe at the University of California, Irvine, describe the dataflow language Id (Irvine dataflow), which is the basis for much later work on dataflow languages. (WPG: Arvind; U-Interpreter; dataflow; Id; University of California (Irvine))

95 : In his Turing Award address, John Backus (inventor of FORTRAN) argues against the use of conventional imperative languages, and for functional programming. The difficulty of programming parallel computers in imperative languages is cited as one argument against them. (WPG: Backus, John; FP; functional programming; dataflow)

96 : CDC demonstrates the Cyber 203, a predecessor of its Cyber 205 product. (LNR: CDC Cyber 203)

97 : Per Brinch Hansen describes remote procedure call (RPC) in paper on distributed processes, although he does not use that term. (AnG: RPC; distributed computing; Brinch Hansen, Per)

98 : Harry F. Jordan describes the Finite Element Machine, later built at NASA Langley, and introduces the term barrier synchronization. (JHF: barrier synchronization; Jordan, Harry F.)

99 : BBN begins design of multiprocessors based around the butterfly switch originally developed for the Pluribus. This switch has its roots in work on perfect-shuffle and Omega networks. (WGV, SHS: BBN Butterfly)

100 : H. T. Kung and Charles Leiserson publish the first paper describing systolic arrays. (LCE: systolic arrays; Kung, H. T.; Leiserson, Charles E.)

101 : Tony Hoare describes the Communicating Sequential Processes (CSP) model. This mixes synchronous point-to-point communication with guarded commands, and is the basis for many later parallel programming languages. (HW: Hoare, Tony; CSP; concurrency)

102 : Steven Fortune and James Wyllie describe the PRAM model, which becomes the standard model for complexity analysis of parallel algorithms. (WGV: Fortune, Steven; Wyllie, James; PRAM)

103 : Leslie Lamport describes the algorithm for creating a partial order on distributed events which bears his name. (WGV: Lamport, Leslie; virtual time)

1979

104 : The first dataflow multiprocessor, with 32 processors, becomes operational at CERT-ONERA in Toulouse, France. (WPG: dataflow; CERT-ONERA)

105 : M. H. Van Emden and G. J. De Lucena at Waterloo propose predicate logic as a language for parallel programming. The authors have great difficulty getting their paper accepted for publication. (RG: logic programming; University of Waterloo)

106 : Josh Fisher at Yale describes trace scheduling, a method of compiling programs written in conventional languages

for wide-word machines. This later becomes the foundation for Multiflow's VLIW systems. (WM: VLIW; trace scheduling; Fisher, Josh; Multiflow; Yale)

107 : IBM's John Cocke designs the 801, the first of what are later called RISC architectures. (KHG: RISC; IBM 801; Cocke, John)

108 : ICL delivers the first DAP to Queen Mary College, London. (WGV: ICL; ICL/AMT DAP)

109 : Inmos set up by British government to develop and produce memory chips and the transputer microprocessor. (WGV: Inmos; transputer)

110 : The first single-processor prototype of the Denelcor HEP becomes operational. (WGV: Denelcor HEP; Smith, Burton)

111 : Parviz Kermani and Leonard Kleinrock describe the virtual cut-through technique for message routing. (WGV: Kermani, Parviz; Kleinrock, Leonard; virtual cut-through; routing)

112 : Level 1 BLAS is released; the LINPACK software package is completed. The LINPACK Users' Guide contains the first LINPACK Benchmark Report, listing performance on 17 machines from the DEC PDP-10 to the Cray 1. The latter achieves 4 MFLOPS for a 100×100 matrix at full precision on a single processor. (DJ: BLAS; standards; LINPACK; benchmarking; CRI CRAY-1)

113 : T. Hoshino, at the University of Kyoto, builds the PAX-9, a disjoint-memory MIMD machine containing 9 Motorola 6800 processors. This machine is the predecessor of later generations of PAX multicomputers built at Tsukuba University to study quantum chromodynamics. (HN: PAX; Hoshino, T.; University of Kyoto; QCD)

1980

114 : PFC (Parallel FORTRAN Compiler) developed at Rice University under the direction of Ken Kennedy. (WM: PFC; Kennedy, Ken; vectorization; Rice University)

115 : Teradata spun off from Citibank to develop parallel database query processors. (WGV: Teradata)

116 : First PS-2000 multiprocessors go into operation in the USSR. Each contains 64 24-bit processing elements on a segmentable bus, with independent addressing in each PE. The machine's total performance is 200 MIPS. Approximately 200 are manufactured between 1981 and 1989. (WcP: PS-2000; IPU; NIIUVM)

117 : J. T. Schwartz publishes paper describing and analyzing the ultracomputer model, in which processors are connected by a shuffle/exchange network. (SHS: Schwartz, J. T.; ultracomputer)

118 : Robin Milner, working at the University of Edinburgh, describes the Calculus of Communicating Systems, a theoretical framework for describing the properties of concurrent systems. (WGV: Milner, Robin; CCS; University of Edinburgh; concurrency)

119 : David Padua and David Kuck at the University of Illinois develop the DOACROSS parallel construct to be used as a target in program transformation. The name DOACROSS is due to Robert Kuhn. (PD: DOACROSS; vectorization; University of Illinois; Padua, David; Kuck, David; program transformation)

120 : DEC develops the KL10 symmetric multiprocessor. Up to three CPUs are supported, but one customer builds a five-CPU system. (FJM: DEC; multiprocessor, symmetric)

121 : First El'brus-1, delivering 12 MIPS, passes testing in the USSR. (WcP: El'brus-1; ITMVT)

122 : Les Valiant describes and analyzes random routing, a method for reducing contention in message-routing networks. The technique is later incorporated into some machines, and is the basis for much work on PRAM emulation. (WGV: Valiant, Les; routing, random)

123 : Burroughs Scientific Processor project cancelled after one sale but before delivery. (WM: Burroughs BSP)

1981

124 : First tagged-token dataflow computer becomes operational at the University of Manchester. (WPG: University of Manchester; dataflow)

125 : Kuck, Kuhn, Padua, Leasure, and Wolfe, at the University of Illinois, describe the use of dependence graphs for vectorization. (ZH: vectorization; Kuck, David; Wolfe, Mike; data dependence)

126 : Floating Point Systems Inc. delivers the first 64-bit FPS-164 array processor, which issues multiple pipelined instructions every cycle. (CBR: FPS FPS-164; array processor; LIW)

127 : Control Data delivers the Cyber 205 vector supercomputer, which has a memory-to-memory architecture. (WM: CDC Cyber 205)

128 : DEC produces the first two-processor VAX 11/782 asymmetric multiprocessor. A small number of 4-processor machines (called the 11/784) are built. (FJM, RP: DEC VAX; multiprocessor, asymmetric)

129 : Bruce J. Nelson, of Xerox PARC and Carnegie-Mellon University, describes and names remote procedure call. RPC is later the basis for many parallel and distributed programming systems. (PDL: RPC; distributed computing; Xerox; CMU)

130 : A group led by Charles Seitz (computer science) and Geoffrey Fox (physics) begins development of a hypercube multicomputer at the Californa Institute of Technology. (WGV: Caltech; hypercube; Seitz, Charles; Fox, Geoffrey)

131 : Danny Hillis writes the first description of the Connection Machine architecture in a memo from the MIT Artificial Intelligence Lab. (BBM: TMC CM-1; Hillis, Danny; MIT)

132 : BBN delivers its first Butterfly multiprocessor. The machine contains Motorola 68000s connected through multistage network to disjoint memories, giving appearance of shared memory. (WGV: BBN Butterfly)

133 : Franco Preparata and Jean Vuillemin describe the cube-connected cycles topology. (WGV: Preparata, Franco; Vuillemin, Jean; cube-connected cycles)

134 : Intel iAPX 432 multiprocessor prototype completed. Intel abandons the project, but some project members later help found companies which pursue the project's ideas. (WGV: Intel iAPX 432)

135 : Silicon Graphics Inc. founded to develop high-performance graphics workstations. (SDE: SGI)

136 : Allan Gottlieb and others describe the NYU Ultracomputer, a shared-memory machine which uses message combining in a multistage interconnection network. (GoA: message combining; NYU Ultracomputer; IBM RP3; Gottlieb, Allan)

1982

137 : Japanese Ministry of International Trade and Industry (MITI) begins the Fifth Generation Computer Systems project, with the aim of building parallel knowledge-based machines using Prolog as a kernel language. Many imitation projects soon begun elsewhere. (RG, MEN: FGCS)

138 : Michael Wolfe's thesis on optimizing compilers for supercomputers appears, It contains the first detailed, coherent account of program transformations for vectorization and shared-memory parallelization. (ZH: Wolfe, Mike; vectorization; parallelization; program transformation; University of Illinois)

139 : Convex (originally called Parsec) founded to pursue mini-supercomputer market. (WGV: Convex)

140 : Steve Chen's group at Cray Research produces the first X-MP, containing two pipelined processors compatible with the CRAY-1 and shared memory. (WGV: CRI CRAY X-MP; Chen, Steve)

141 : Hitachi introduces its S-810 vector supercomputers, with peak rates up to 800 MFLOPS. (OY, HN: Hitachi S-810)

142 : ILLIAC-IV decommissioned. (WGV: ILLIAC-IV)

143 : Alliant (originally named Dataflow) founded to built mini-supercomputers. (WGV, WM: Alliant)

144 : First Denelcor HEPs installed in US. A total of eight machines are eventually built. (WGV: Denelcor HEP)

145 : T. Hoshino, at Kyoto University, builds the PAX-32 and PAX-128, containing 32 and 128 Motorola 68000 processors respectively. (HN: PAX; Hoshino, T.; University of Tsukuba; QCD)

146 : Control Data improves its Flexible Processor to create the Advanced Flexible Processor (AFP), with a 210-bit instruction word. (WM, ND: CDC Flexible Processor; CDC AFP)

147 : Fujitsu ships its first VP-200 vector supercomputer, with a peak rate of 500 MFLOPS. (OY, HN: Fujitsu VP-200)

148 : Sperry Univac delivers the first 1100/80 machines. Each contains up to four CPUs, four I/O processors, and two array processor subsystems. Pacific-Sierra Research (PSR) develops the VAST parallelizing tool to help translate DO-loops into parallel operations. (FRM: UNIVAC 1100/80; array processor; PSR)

149 : Japanese MITI begins a ten-year Superspeed project, whose goal is a 10 GFLOPS supercomputer. (RG, MEN: Superspeed)

150 : Cosmic Cube hypercube prototype goes into operation at Caltech. The first predecessor of the CrOS (Crystalline Operating System) programming system is developed. (WGV: Caltech; hypercube; CrOS; message passing)

1983

151 : Loral Instrumentation begins development of the Loral DataFlo computer. (VZJ: Loral LDF-100; Van Zandt, John; dataflow)

152 : J. R. Allen's Ph.D. thesis at Rice University introduces the concepts of loop-carried and loop-independent dependencies, and formalizes the process of vectorization. (ZH: data dependence; vectorization; Rice University)

153 : Ada reference manual published by the US Department of Defence. The language introduces rendezvous mechanism for interprocess communication and synchronization, and is widely criticized for its complexity. (AnG: Ada; rendezvous)

154 : Scientific Computer Systems founded to design and market Cray-compatible minisupercomputers. (WM: SCS)

155 : ETA Systems, Inc. spun off from CDC to develop a new generation of vector supercomputers. (WGV: CDC; ETA)

156 : NEC introduces its SX-1 vector supercomputer. (OY: NEC SX-1)

157 : DEC modifies its popular VMS operating system to support loosely-coupled clusters of VAXes. (FJM: DEC VAX; multiprocessor, symmetric)

158 : The full Mark I Cosmic Cube hypercube goes into operation at Caltech. Work begins on its successor, the Mark II. (WGV, KV: Caltech; hypercube)

159 : Sheryl Handler and Danny Hillis found Thinking Machines Corporation; Hillis' Ph.D. thesis is used as a starting point for a massively-parallel AI supercomputer. (BBM: TMC; Hillis, Danny; Handler, Sheryl)

160 : Impressed by the Caltech hypercubes, Steve Colley and John Palmer leave Intel to found nCUBE. (WGV, KV: Caltech; nCUBE; Colley, Steve; Palmer, John)

161 : CRAY-1 with 1 processor achieves 12.5 MFLOPS on the 100×100 LINPACK benchmark. (DJ: LINPACK; benchmarking; CRI CRAY-1)

162 : The US Defence Advanced Research Projects Agency (DARPA) starts the Strategic Computing Initiative, which helps fund such machines as the Thinking Machines Connection Machine, BBN Butterfly, and CMU WARP (later Intel iWARP). (WM: DARPA)

163 : SISAL (Streams and Iterations in a Single-Assignment Language) language definition released by Lawrence Livermore National Laboratory (LLNL), Colorado State University, DEC, and University of Manchester. A descendent of dataflow languages, it includes array operations, streams, and iterations. (FJ: SISAL; functional programming; dataflow; LLNL; DEC; University of Manchester; CSU)

164 : David May publishes first description of Occam, a concurrent programming language based on CSP which is closely associated with the transputer. (SR: Occam; May, David; programming languages; CSP)

165 : Tandem ships its Fiber Optic Extension (FOX) ring network to connect distributed clusters of processors. Several systems containing more than 100 processors are built. (HB: Tandem; ring network; fiber optics; distributed computing)

166 : Goodyear Aerospace delivers the Massively Parallel Processor (MPP) to NASA Goddard. The Machine contains 16K processors in a 128×128 grid, each with 1024 bits of memory. (WM: Goodyear MPP; NASA Goddard)

167 : Myrias Research spun off from University of Alberta to build shared-memory mini-supercomputers. (WGV: Myrias)

168 : Sequent founded. Several of its founders are former members of Intel iAPX 432 project. (WGV, LT: Sequent; Intel iAPX 432)

169 : Encore founded to build mini-supercomputers. (WGV: Encore)

1984

170 : Ron Cytron's Ph.D. thesis at the University of Illinois extends the concept of DOACROSS loops. (ZH, PD: Cytron, Ron; DOACROSS; vectorization; University of Illinois)

171 : Harry F. Jordan implements The Force, the first SPMD programming language, on the Denelcor HEP. (JHF: Jordan, Harry F.; programming languages; The Force; Denelcor HEP)

172 : The CRAY X-MP family is expanded to include 1- and 4-processor machines. A CRAY X-MP running CX-OS, the first Unix-like operating system for supercomputers, is delivered to NASA Ames. (WGV, MEN: CRI CRAY X-MP; NASA Ames)

173 : Intel Scientific Computers is set up by Justin Rattner to produce hypercube multicomputers commercially. (WGV: Intel; hypercube; Rattner, Justin)

174 : Sequent produces its first shared-memory Balance multiprocessors, using NS32016 microprocessors and a proprietary Unix-like symmetric operating system called DYNIX. (WGV, LT: Sequent Balance)

175 : Center for Supercomputing Research and Development (CSRD) founded at the University of Illinois. Work begins on CEDAR, a hierarchical shared-memory machine. (PD: University of Illinois; Cedar; CSRD)

176 : Cydrome founded by B. R. Rau and others to build VLIW mini-supercomputers with architectural support for software pipelining of loops. (RR: Cydrome; VLIW; software pipelining; Rau, B. R.)

177 : Mitsui Shipbuilding Company installs a toroidal multicomputer called the PAX-64J at the University of Tsukuba. (OY: University of Tsukuba; Mitsui PAX-64J)

178 : CRAY X-MP with 1 processor achieves 21 MFLOPS on 100×100 LINPACK. (DJ: LINPACK; benchmarking; CRI CRAY X-MP)

179 : Robert Halstead at MIT introduces and names the futures construct in a paper describing the implementation of Multilisp. (WGV, HR: Multilisp; Halstead, Robert; futures; MIT; functional programming)

180 : Unimpressed with available commercial machines, Caltech begins work on Mark III hypercube. (WGV: Caltech; hypercube)

181 : Multiflow founded by Josh Fisher and others from Yale to produce very long instruction word (VLIW) supercomputers. (WGV: Multiflow; Fisher, Josh)

182 : Work starts on Level 2 of the BLAS software. (DCJ: BLAS-2)

1985

183 : David Gelernter at Yale publishes a description of Linda. Key elements of it later re-appear in the Linda parallel programming system. (WGV: Gelernter, David; Linda; Yale; programming languages)

184 : Convex delivers the first of its single-processor C1 mini-supercomputers using a custom VAX-like vector processor. (WM, SDH: Convex C1)

185 : Cray Research produces the CRAY-2, with four background processors, a single foreground processor, a 4.1 nsec clock cycle, and 256 Mword memory. The machine is cooled by an inert fluorocarbon previously used as a blood substitute. (WGV, MEN, SD: CRI CRAY-2)

186 : Fujitsu introduces its VP-400 vector supercomputer. (OY: Fujitsu VP-400)

187 : Intel produces the first iPSC/1 hypercube, which contains 80286 processors connected through Ethernet controllers. (WGV: Intel iPSC/1; hypercube)

188 : IBM introduces the 3090 vector processor. (KHG: IBM 3090)

189 : W. K. Giloi's design is chosen as the basis for the German Suprenum supercomputer project. (SM: SUPRENUM; Giloi, W. K.)

190 : Thinking Machines Corporation demonstrates first CM-1 Connection Machine to DARPA. (BBM: TMC CM-1)

191 : Inmos produces first (integer) T414 transputer. Members of the implementation group leave to found Meiko, which demonstrates its first transputer-based Computing Surface that year. Parsytec founded in Germany to build transputer-based machines; ESPRIT Supernode project begins work on floating-point transputer. (WGV, RC: Inmos; transputer; Supernode; Meiko; Parsytec)

192 : Alliant delivers its first FX/8 vector multiprocessor machines. The processors are a custom implementation of an extended Motorola 68020 instruction set. An auto-parallelizing FORTRAN compiler is shipped with the machine. (PSC: Alliant FX/8; parallelization)

193 : Denelcor closes doors. (WGV: Denelcor)

194 : Dally and Seitz develop the wormhole routing model, invent virtual channels, and show deadlock-free routing can be performed using virtual channels. (DW: Dally, Bill; Seitz, Charles; routing, wormhole; virtual channels)

195 : A 16-node QCD machine at Columbia University begins operation. The machine delivers 250 MFLOPS peak and 60 MFLOPS sustained performance. (CNH: Columbia University; QCD)

196 : NEC SX-2 with 1 processor achieves 46 MFLOPS on 100×100 LINPACK. (DJ: LINPACK; benchmarking; NEC SX-2)

197 : Supertek Computers, Inc. is founded by Mike Fung, a former Hewlett Packard RISC project manager. (WGV: Supertek)

198 : NEC delivers its SX-2 vector supercomputer. The machine has a 6.0 ns clock,

is capable of producing 8 floating point results per clock cycle, and can be configured with up to 256 MByte of memory. (TPD: NEC SX-2)

199 : Teradata ships the first of its DBC/1012 parallel database query engine. These machines contain Intel 8086 processors connected by proprietary tree network. (WGV: Teradata DBC/1012)

200 : ICL produces a 1024-processor MiniDAP for use as workstation co-processor. (VDBS: ICL; ICL/AMT DAP)

201 : nCUBE produces the first of its nCUBE/10 hypercube multicomputers using custom VAX-like processors. (WGV: nCUBE nCUBE/10; hypercube)

202 : Charles Leiserson describes the fat-tree network. (LCE: fat tree; routing; Leiserson, Charles E.)

203 : David Jefferson describes how virtual time and time warping can be used as a basis for speculative distributed simulations. (WGV: Jefferson, David; timewarp; discrete event simulation)

204 : IBM begins the RP3 project, to build a scalable shared-memory multiprocessor using a message-combining switch similar to that in the NYU Ultracomputer. (KHG: IBM RP3; NYU Ultracomputer; message combining)

205 : Pfister and Norton analyze hot spot contention in multistage networks, and describe how message combining can ameliorate its effects. (WGV: Pfister, Gregory; Norton, V. A.; hot spots; message combining)

1986

206 : Loral Instrumentation delivers the first LDF-100 dataflow computer to the U.S. government. Two more systems are shipped before the project is shut down. (VZJ: Loral LDF-100; Van Zandt, John; dataflow)

207 : Gul Agha, at the University of Illinois, describes a new form of the Actors model which is the foundation for much later work on fine-grained multicomputer architectures and software. (AgG: Agha, Gul; Actors)

208 : The CrOS III programming system, Cubix (a file-system handler) and Plotix (a graphics handler) are developed for the Caltech hypercubes. These are later the basis for several widely-used message-passing programming systems. (WGV: hypercube; CrOS)

209 : Scientific Computer Systems delivers first SCS-40, a Cray-compatible minisupercomputer. (WGV: SCS SCS-40)

210 : First El'brus-2 completed in the USSR. The machine contains 10 processor, and delivers 125 MIPS (94 MFLOPS) peak performance. Approximately 200 machines are later manufactured. (WcP: El'brus-2; ITMVT)

211 : Thinking Machines ships first CM-1 Connection Machine, containing up to 65536 single-bit processors connected in hypercube. (WGV: TMC CM-1; data parallelism)

212 : Encore ships its first bus-based Multimax computer, which couples NS32032 processors to Weitek floating-point accelerators. (WGV: Encore; Encore Multimax)

213 : Dally shows that low-dimensional k-ary n-cubes are more wire-efficient than

hypercubes for typical values of network bisection, message length, and module pinout. Dally demonstrates the torus routing chip, the first low-dimensional wormhole routing component. (DW: Dally, Bill; k-ary n-cubes; hypercube; routing, wormhole; Caltech)

214 : Kai Li describes system for emulating shared virtual memory on disjoint-memory hardware. (WGV: Li, Kai; shared virtual memory)

215 : The Universities of Bologna, Padua, Pisa, and Rome, along with CERN and INFN, complete a 4-node QCD machine delivering 250 MFLOPS peak and 60 Mflops sustained performance. (CNH: APE; University of Rome; QCD)

216 : CRAY X-MP with 4 processors achieves 713 MFLOPS (against a peak of 840) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; CRI CRAY X-MP)

217 : Alan Karp offers $100 prize to first person to demonstrate speedup of 200 or more on general purpose parallel processor. Benner, Gustafson, and Montry begin work to win it, and are later awarded the Gordon Bell Prize. (KA: Karp Prize; Karp, Alan)

218 : Arvind, Nikhil, and Pingali at MIT propose the I-structure, a parallel array-like structure allowing side effects. This is incorporated into the Id language, and similar constructs soon appear in other high-level languages. (BDA, HR: Arvind; I-structure; Id; functional programming; dataflow; MIT)

219 : Floating Point Systems introduces its T-series hypercube, which combines Weitek floating-point units with Inmos transputers. A 128-processor system is shipped to Los Alamos. (CBR: FPS T-series; transputer; LANL)

220 : Active Memory Technology spun off from ICL to develop DAP products. (WGV: AMT; ICL; ICL/AMT DAP)

221 : Kendall Square Research Corporation (KSR) is founded by Henry Burkhardt (a former Data General and Encore founder) and Steve Frank, to build multiprocessor computers. (WGV: KSR; Burkhardt, Henry)

222 : GE installs a prototype 10-processor programmable bit-slice systolic array called the Warp at CMU. (RJR: CMU; GE; Warp; CMU; systolic arrays)

1987

223 : Chuan-Qi Zhu and Pen-Chung Yew at CSRD describe algorithms for run-time data dependence testing. These influence the implementation of synchronization primitives on the Cedar multiprocessor. (PD: loop scheduling; CSRD; Cedar)

224 : Piyush Mehrotra and John Van Rosendale describe BLAZE, a language for shared-memory systems. The compiler uses data distribution descriptions in its intermediate form. (ZH, MP: BLAZE; data distribution; programming languages; Mehrotra, Piyush; Van Rosendale, John)

225 : ParaSoft spun off from hypercube group at Caltech to produce commercial version of CrOS-like message-passing system. (WGV: Caltech; Express; ParaSoft; hypercube; CrOS; message passing)

226 : ETA produces first air- and liquid nitrogen-cooled versions of ETA^{10}

multiprocessor supercomputer. Principal architect is Neil Lincoln. (WGV: ETA ETA-10; Lincoln, Neil)

227 : Intel produces the iPSC/2 hypercube using the 80386/7 chip-set and circuit-switched routing. The machine includes concurrent I/O facilities. (WGV, TB, WoP: Intel iPSC/2)

228 : Sequent produces its 80386-based Symmetry bus-based multiprocessor. (WGV, LT: Sequent Symmetry)

229 : The Caltech Mark III hypercube completed. The machine uses Motorola 68020 microprocessors and wormhole routing. (WGV: Caltech; hypercube)

230 : Thinking Machines Corporation introduces the CM-2 Connection Machine, which contains 64k single-bit processors connected in hypercube and 2048 Weitek floating point units. The machine's first FORTRAN compiler is developed by Compass Inc. (WGV, PDL: TMC CM-2; data parallelism; Compass)

231 : Parsytec delivers its first transputer-based SuperCluster machine. (RC: Parsytec; Parsytec SuperCluster)

232 : Myrias produces a prototype 68000-based SPS-1 multiprocessor. The machine emulates shared memory at the operating system level. (WGV: Myrias SPS-1)

233 : Cydrome delivers the first Cydra 5. The machine contains a single VLIW numeric processor with a 256-bit instruction word capable of 7 operations per cycle, and multiple scalar processors for I/O and general-purpose work. (RR: VLIW; Cydrome Cydra 5)

234 : J. van Leuwen and R. B. Tan describe interval routing, a compact way of encoding distributed routing information for many topologies. This is later used in the Inmos T9000 transputer. (RE: routing, interval; transputer)

235 : V. Nageshwara Rao and Vipin Kumar propose the use of isoefficiency to assess the scalability of parallel algorithms. (WGV: isoefficiency; scalability; performance metrics)

236 : Second-generation QCD machine containing 64 nodes goes into operation at Columbia
University, delivering 1 GFLOPS peak and 300 MFLOPS sustained performance. (CNH: Columbia University; QCD)

237 : ETA^{10} with 1 processor achieves 52 MFLOPS on 100×100 LINPACK; NEC SX-2 with 1 processor achieves 885 MFLOPS (against a peak of 1300) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; ETA ETA-10; NEC SX-2)

238 : The first Gordon Bell Prizes for parallel performance is awarded. The recipients are Brenner, Gustafson, and Montry, for a speedup of 400-600 on variety of applications running on a 1024-node nCUBE, and Chen, De Benedictis, Fox, Li, and Walker, for speedups of 39-458 on various hypercubes. (WGV: Gordon Bell Prize; Bell, Gordon)

239 : AMT delivers the first of its re-engineered DAPs, with 1024 single-bit processors connected in torus. (WGV, VDBS: AMT; ICL/AMT DAP)

240 : Multiflow delivers the first Trace/200 VLIW machines, which use 256 to 1024 bits per instruction. (WGV: Multiflow Trace/200; VLIW)

241 : Charles Seitz, working at Ametek, builds the Ametek-2010, the first parallel computer using a 2-D mesh interconnect with wormhole routing. (DW: Seitz, Charles; Ametek Ametek-2010; routing, wormhole)

242 : Abhiram Ranade describes how message combining, butterfly networks, and a complicated routing algorithm can emulate PRAMs in near-optimal time. (WGV: Ranade, Abhiram; butterfly; PRAM emulation)

243 : Work starts on Level 3 BLAS. The LAPACK project is begun, with the aim of producing linear algebra software for shared memory parallel computers. (DJ, DCJ: BLAS-3; LAPACK)

1988

244 : The 128 processing-element SIGMA-1 dataflow machine of Japan's Electro-Technical Laboratory (ETL) delivers over 100 MFLOPS. (WPG: dataflow; SIGMA-1; ETL)

245 : Ian Foster and Stephen Taylor describe Strand, a parallel programming language based on logic programming. Strand Software Technologies produces a commercial version called Strand88. (FIT: logic programming; Strand88)

246 : Hans Zima, Heinz Bast, and Hans Michael Gerndt describe SUPERB, the first automatic parallelization system for disjoint-memory computers. Ken Kennedy and David Callahan describe many of the same ideas in a paper published later the same year. (WGV: Zima, Hans; Kennedy, Ken; parallelization; SUPERB)

247 : Piyush Mehrotra and John Van Rosendale describe Kali, the first language allowing user-specified data distributions on MIMD machines. Many of these ideas later appear in Vienna FORTRAN and HPF. (MP: Kali; data distribution; programming languages; Mehrotra, Piyush; Van Rosendale, John)

248 : ParaSoft releases the first commercial version of its Express message-passing system. (WGV: ParaSoft; Express; Caltech; DIME)

249 : Convex introduces its second-generation C2 mini-supercomputers, which use some gallium arsenide gate arrays. Each machine could contain 1, 2, or 4 processors. (SDH, PJA: Convex C2; GaAs)

250 : CRI produces the first of its Y-MP multiprocessor vector supercomputers. (WGV: CRI CRAY Y-MP)

251 : Intel begins delivering iPSC/2 hypercubes incorporating wormhole routing. (WoP: Intel iPSC/2)

252 : Silicon Graphics produces its first Power Series bus-based multiprocessor workstations, with up to 8 MIPS R2000 RISC microprocessors each. (SDE: SGI Power Series)

253 : Work begins at Indian Centre for Development of Advanced Computing (CDAC) on a transputer-based parallel machine called PARAM. (DRV: PARAM; transputer; CDAC)

254 : Thinking Machines Corporation introduces the DataVault mass storage subsystem, which uses up to 84 small disks to achieve high bandwidth and fault tolerance. (BBM: TMC DataVault; mass storage)

255 : Inmos produces the first T800 floating-point transputer; Meiko and Parsytec begin marketing T800-based machines. (WGV: Inmos; transputer; Parsys; Telmat; Meiko; ESPRIT Supernode)

256 : Cydrome closes doors. (RR: Cydrome)

257 : John Gustafson and Gary Montry argue that Amdahl's Law can be invalidated by increasing problem size. (WGV: scalability; Gustafson's Law; Amdahl's Law)

258 : Friedemann Mattern and Colin Fidge develop implementations of Lamport's partially-ordered virtual time algorithm for distributed systems. (FCJ: virtual time)

259 : The Universities of Bologna, Padua, Pisa, and Rome, along with CERN and INFN, complete a 16-node QCD machine delivering 1 GFLOPS peak and 300 Mflops sustained performance. (CNH: APE; University of Rome; QCD)

260 : CRAY Y-MP with 1 processor achieves 74 MFLOPS on 100×100 LINPACK; the same machine with 8 processors achieves 2.1 GFLOPS (against a peak of 2.6) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; CRI CRAY Y-MP)

261 : Gordon Bell Prize awarded to Vu, Simon, Ashcraft, Grimes, and Peyton, whose static structures program achieves 1 GFLOPS on an 8-processor CRAY Y-MP. (WGV: Gordon Bell Prize)

262 : Rosing and Schnabel describe DINO, an extension to C for describing processor structures and data distributions for distributed-memory machines. (ZH: data distribution; programming languages)

263 : Floating Point Systems Inc. changes its name to FPS Computing and buys Celerity Computing. The reformed company produces the Model 500 (Celerity 6000) mini-supercomputer with multiple scalar and vector processors. (CBR: FPS; Celerity; FPS Model 500)

264 : MasPar Computer Corp. founded by former DEC executive Jeff Kalb to develop massively-parallel SIMD machines. (WM: DEC; MasPar; data parallelism; Kalb, Jeff)

265 : Tera Computer Co. founded by Burton Smith and James Rottsolk to develop and market a new multi-threaded parallel computer, similar to the Denelcor HEP. (KLS: Tera; Smith, Burton)

266 : Scalable Coherent Interface (SCI) working group formed to develop standard for interconnection network providing 1 GByte per second per processor and cache coherence using many unidirectional point-to-point links. (GDB: SCI)

267 : Mirchandaney, Saltz, Smith, Nicol and Crowley describe and implement the inspector/executor method for run-time pre-processing of loops with irregular data accesses, along with a scheme for implementing user-defined, compiler-embedded partitions. (SaJ: data distribution; loop scheduling)

268 : Patterson, Gibson, and Katz describe the use of redundant arrays of inexpensive disks (RAID) for mass storage. (WGV, OJ: RAID; mass storage)

1989

269 : Murray Cole, at the University of Edinburgh, proposes the use of algorith-

mic skeletons as a basis for parallel functional programming. (BDA: Cole, Murray; skeletons; University of Edinburgh)

270 : A prototype of the SUPERB automatic parallelization system finished. Developed as part of the German SUPRENUM project, this translated FORTRAN 77 programs annotated with data distribution specifications into code containing explicit message-passing. A vectorizing FORTRAN 77 compiler is developed by Compass Inc. (ZH, PDL: SUPERB; vectorization; parallelization; SUPRENUM; Compass)

271 : Scientific Computer Systems stops selling its SCS-40 Cray-compatible computer system. SCS continues to sell high-speed token ring network. (WM: SCS)

272 : Control Data shuts down ETA Systems in April. (WM: CDC; ETA)

273 : Fujitsu begins production of single-processor VP-2000 vector supercomputers. (WGV: Fujitsu VP-2000)

274 : Evans and Sutherland, builders of high-performance graphics systems, announce the ES-1 parallel computer. Two systems are delivered before the division is shut down. (WM: Evans and Sutherland ES-1)

275 : Meiko begins using SPARC and Intel i860 processors to supplement T800s in its Computing Surface machines. (WGV: Meiko Computing Surface)

276 : BBN delivers its first 88000-based TC2000 multiprocessor, a descendent of the Butterfly series of machines. (WGV: BBN TC2000)

277 :
Multiflow produces its second-generation Trace/300 VLIW machines. (WM: Multiflow Trace/300; VLIW)

278 : Les Valiant argues that random routing and latency hiding can allow physically-realizable machines to emulate PRAMs optimally, and proposes the bulk-synchronous model as an intermediate between software and hardware. (WGV: Valiant, Les; routing, random; PRAM emulation)

279 : Third-generation QCD machine containing 256 nodes goes into operation at Columbia University, delivering 16 GFLOPS peak and 6.4 GFLOPS sustained performance. (UL, CNH: Columbia University; QCD)

280 : CRAY Y-MP with 8 processors achieves 275 MFLOPS on 100×100 LINPACK, and 2.1 GFLOPS (against a peak of 2.6) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; CRI CRAY Y-MP)

281 : Gordon Bell Prize for absolute performance awarded to a team from Mobil and Thinking Machines Corporation, who achieve 6 GFLOPS on a CM-2 Connection Machine; prize in price/performance category awarded to Emeagwali, who achieves 400 MFLOPS per million dollars on the same platform. (WGV: Gordon Bell Prize)

282 : Supertek Computers, Inc., delivers its S-1 Cray-compatible minisupercomputer; 10 of these are eventually sold. (WM: Supertek S-1)

283 : Seymour Cray leaves Cray Research to found Cray Computer Corporation. (WGV: CRI; CCC; Cray, Seymour)

284 : National Aerospace Laboratory (NAL) begins feasibility study on Numerical

Wind Tunnel in conjunction with Fujitsu, Hitachi, and NEC. (HN: Numerical Wind Tunnel; NAL)

285 : Myrias sells its first 68020-based SPS-2 shared-memory multiprocessor. (WGV: Myrias SPS-2)

286 : Guy Blelloch describes the scan-vector model of data parallelism, which relies heavily on the parallel prefix operation. (WGV: Blelloch, Guy; scan-vector model; data parallelism)

287 : nCUBE produces its second-generation nCUBE/2 hypercubes, again using custom processors. (WM: nCUBE nCUBE/2)

1990

288 : Charles Koelbel's Ph.D. thesis at Purdue describes a methodology for automatically generating message-passing code from data distribution directives in Kali programs. The compiler is the first to support both regular and irregular computations using the inspector/executor strategy. (ZH, MP: Kali; data distribution; programming languages; HPF; Koelbel, Charles; Purdue University)

289 : Cray Research, Inc., purchases Supertek Computers Inc., makers of the S-1, a minisupercomputer compatible with the CRAY X-MP. (WM: CRI; Supertek)

290 : NEC ships SX-3, the first Japanese parallel vector supercomputer. Each machine contains up to 4 processors, each with up to 4 pipeline sets, uses a 2.9 ns clock, and has up to 4 Gbyte of memory. (TPD: NEC SX-3)

291 : Intel begins producing iPSC/860 hypercubes, using its i860 microprocessor and circuit-switched connections. (JR, TB: Intel iPSC/860)

292 : DEC announces and delivers the VAX 9000, a shared memory vector processor running the VMS operating system. (MEN: DEC VAX; Trilogy; Amdahl, Gene)

293 : 4-cluster 32-processor Cedar multiprocessor becomes fully functional at CSRD. (PD: University of Illinois; Cedar; CSRD)

294 : First MasPar MP-1 delivered. Each contains up to 16k 4-bit processors connected by both 8-way mesh and circuit-switched crossbar. The FORTRAN compiler is developed by Compass Inc. (BJD, WGV: Maspar MP-1; Compass)

295 : Myrias sells the first of its second-generation 68040-based SPS-3 shared-memory multiprocessors. (KWT: Myrias SPS-3)

296 : Multiflow closes doors. (WM: Multiflow)

297 : Intel demonstrates its iWarp systolic array, a descendent of Warp using custom microprocessor instead of wire-wrapped boards. (RJR: Intel iWarp; systolic arrays; CMU)

298 : University of Tsukuba completes a 432 processor machine called QCDPAX in collaboration with Anritsu Corporation. (OY: QCDPAX; Anritsu; University of Tsukuba)

299 : Fujitsu VP-2600 with 1 processor achieves 2.9 GFLOPS (against a peak of 5 GFLOPS) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; Fujitsu VP-2600)

300 : Gordon Bell Prize in price/performance category awarded to Geist, Stocks, Ginatempo, and Shelton, who achieves 800 MFLOPS per million dollars in a high-temperature superconductivity program on a 128-node Intel iPSC/860. The prize in the compiler parallelization category is awarded to Sabot, Tennies, and Vasilevsky, who achieve 1.5 GFLOPS on a CM-2 Connection Machine with FORTRAN 90 code derived from FORTRAN 77. (WGV: Gordon Bell Prize)

301 : National Energy Research Supercomputer Center (NERSC) at LLNL places order with Cray Computer Corporation for CRAY-3 supercomputer. The order includes a unique 8-processor CRAY-2 computer system that is installed in April. (WM: CCC CRAY-3; LLNL)

302 : Fujitus ships the first of its VP-2600 vector supercomputer. (OY: Fujitsu VP-2600)

303 : Fujitsu, Hitachi, and NEC build a testbed parallel vector supercomputer using four Fujitsu VP-2600s, NEC's shared memory, and Hitachi software. This machine is the result of the Superspeed project begun in 1982. (OY: Fujitsu; NEC; Hitachi)

304 : Alliant delivers the first of its FX/2800 i860-based multiprocessors. (WGV: Alliant FX/2800)

305 : Wavetracer builds the DTC (Data Transport Computer) consisting of one to four boards of 16×16×16 1-bit PEs. It is the first three-dimensional array processor. (SMC: Wavetracer DTC)

306 : Level 3 BLAS published/released. The Parallel Virtual Machine (PVM) project is started to develop software needed to use heterogeneous distributed computers. (DJ: BLAS-3; PVM)

307 : The two ETA^{10} systems at the closed John von Neumann Supercomputer Center are destroyed with sledge hammers, in order to render them useless, after no buyers are found. (WM: ETA ETA-10)

308 : Fujitsu begins producing the AP1000, containing 64 to 512 SPARC processors connected by a point-to-point toroidal network, a global broadcast tree, and a synchronization bus. (LH: Fujitsu AP1000)

309 : MIT's J-Machine project demonstrates a message-driven network interface that reduces overhead of message handling. (DW: Dally, Bill; J-Machine; Actors; MIT)

1991

310 : OSC 12.0 SISAL compiler is released by LLNL and CSU. First functional language compiler for multiprocessor vector supercomputers. SISAL programs achieve FORTRAN speeds on the CRAY X-MP and CRAY Y-MP supercomputers. (FJ: SISAL; functional programming; dataflow; LLNL; CSU)

311 : Bill Pugh, at the University of Maryland, describes the Omega test for data dependence analysis of loops. (WM: vectorization; data dependence; Omega test; University of Maryland)

312 : Jingke Li and Marina Chen describe a systematic approach for specifying communication and optimizing an automatic mapping from access patterns to communication structures. They later obtain the first NP-completeness result for the

alignment problem. (ZH, LJ: data distribution; CRYSTAL; Chen, Marina; Li, Jingke)

313 : Applied Parallel Research (APR) spun off from Pacific-Sierra Research (PSR) to develop FORGE and MIMDizer parallelization tools, and to upgrade them to handle FORTRAN 90. (BBM, WG: APR; APR FORGE; APR MIMDizer; PSR)

314 : Convex ships its first C3 supercomputer, using gallium arsenide components. Each machine contains up to 8 vector processors. (SDH: Convex C3; GaAs)

315 : CRI produces first Y-MP C90. (WGV: CRI CRAY Y-MP C90)

316 : Intel begins marketing iWarp systolic array systems, featuring an LIW processor with on-chip communication, low-latency communication, and 512 kbyte to 2 Mbyte per processor. (RJR: Intel iWarp; systolic arrays)

317 : Sun begins shipping the SPARCserver 600 (also called Sun-4/600) series machines (shared-memory multiprocessors containing up to 4 SPARC CPUs each). (DPC: Sun; multiprocessor)

318 : A PARAM supercomputer containing 256 T800 transputers connected in four 64-node clusters by 96×96 crossbars begins running at India's CDAC. Alternative machine configuration containing i860s are also developed; machines are later sold to Germany, Russia, and Canada. (DRV: PARAM; transputer; CDAC)

319 : Thinking Machines Corporation produces CM-200 Connection Machine, an upgraded CM-2. (BBM: TMC CM-200)

320 : Meiko produces a commercial implementation of the ORACLE Parallel Server database system for its SPARC-based Computing Surface systems. (AT: Meiko Computing Surface; Oracle)

321 : Myrias closes doors. (WGV: Myrias)

322 : José Duato describes a theory of deadlock-free adaptive routing which works even in the presence of cycles within the channel dependency graph. (RE: routing, adaptive)

323 : A 256-node QCD machine begins operation at Fermilab, delivering 5 GFLOPS peak and 1 GFLOPS sustained performance. (CNH: ACPMAPS; Fermilab; QCD)

324 : CRAY Y-MP C90 with 16 processors achieves 403 MFLOPS on 100×100 LINPACK; a Fujitsu VP-2600 with 1 processor achieves 4 GFLOPS (against a peak of 5 GFLOPS) on 1000×1000 LINPACK. (DJ: LINPACK; benchmarking; CRI CRAY Y-MP C90; Fujitsu VP-2600)

325 : David Bailey publishes a complaint about the abuse of benchmark figures, particularly by parallel computer vendors. (WGV: Bailey, David; benchmarking)

326 : Geoffrey Fox, Ken Kennedy, and others describe FORTRAN D, a language extension for distributed-memory systems. This is later one of the parents of High Performance FORTRAN (HPF). (ZH: FORTRAN D; HPF; Kennedy, Ken; Fox, Geoffrey)

327 : FPS Computing delivers the MCP-784, an 84-processor shared-memory system using Intel i860 microprocessors. (CBR: FPS MCP-784)

328 : NERSC cancels its contract to buy a CRAY-3 from Cray Computer Corp. (WM: CCC CRAY-3; LLNL)

329 : Intel delivers the Touchstone Delta prototype for its Paragon multicomputer, which uses a two-dimensional mesh of i860 microprocessors with wormhole routing, to the Concurrent Supercomputing Consortium at Caltech. Commercial deliveries of Paragon begin later in the year. (JR: Intel Paragon; routing, wormhole; Caltech)

330 : Germany's SUPRENUM project produces its first bug-free hardware using clusters of nodes based on Motorola 68020 with Weitek vector processors. No further hardware is built, as the technology used is no longer competitive. (SM: SUPRENUM)

331 : Thinking Machines Corporation announces the CM-5 Connection Machine, a MIMD machine containing a fat-tree of SPARCs, each of which incorporates up to four custom vector processors manufactured by TI. First machine installed at Minnesota Supercomputer Center later that year. (BBM, BEA: TMC CM-5; fat tree; TI; MSC)

332 : BBN shuts down its Advanced Computers, Inc. subsidiary, though it continues to sell TC-2000 computers. (WM: BBN)

333 : AMT adds 8-bit arithmetic co-processors to the processing elements in its DAP products. (VDBS: AMT; ICL/AMT DAP)

334 : Kendall Square Research starts to deliver 32-node KSR-1 multiprocessors. The machines use a cache-only memory architecture, with nodes connected in a high-speed ring. (WM: KSR KSR-1)

335 : 64-processor nCUBE 2 with 48 I/O processors and 205 disks achieves 1073 transactions per second running Oracle Parallel Server—twice the speed of the fastest contemporary mainframe, at one-twentieth the cost per transaction. (BJ, KV: nCUBE; Oracle)

1992

336 : The Japanese Fifth Generation Computer System project completes its 10-year research program, and puts its software into the public domain. (RG: logic programming; FGCS)

337 : Benkner, Brezany, Chapman, Mehrotra, Schwald, and Zima describe Vienna FORTRAN and Vienna FORTRAN 90, dialects of FORTRAN containing explicit data distribution directives. (ZH: Zima, Hans; Vienna FORTRAN)

338 : Message-Passing Interface Forum (MPI) formed to define standard for message-passing systems for parallel computers. (HT, GI: MPI; standards; message passing)

339 : FPS Computing closes doors. Selected assets are bought by CRI, which forms a Cray Research Superservers (CRS) subsidiary formed. The FPS Model 500 is renamed the Cray S-MP, and the FPS MCP is renamed the Cray APP. (CBR: FPS; CRI)

340 : AMT closes doors, but is revived as Cambridge Parallel Processing. (WM: AMT; Cambridge Parallel Processing)

341 : Meiko deliver the first CS-2 Computing Surface to the University of Southampton. The machine is a fat-tree of SPARC processors, each of which is coupled to

a SPARC-like network interface chip and a Fujitsu μVP vector processor. (AT: Meiko CS-2; University of Southampton; Fujitsu μVP)

342 : Alliant closes doors. (MLF: Alliant)

343 : Ultra III Ultracomputer prototype begins operation at NYU. This machine is the first to do asynchronous message combining in hardware. (GoA: message combining; NYU Ultracomputer)

344 : 64-processor DASH multiprocessor in operation at Stanford. Machine runs multi-threaded Unix operating system. (GuA: DASH; multiprocessor; Stanford University)

345 : LAPACK software released. ScaLAPACK Project begins work on providing linear algebra software for highly parallel systems. (DJ: LAPACK; ScaLAPACK)

346 : CRAY Y-MP C90 with 16 processors achieves 479 MFLOPS on 100×100 LINPACK; an NEC SX-3/44 with 4 processors achieves 13.4 GFLOPS (against a peak of 22.0) on 1000×1000 LINPACK, and 20.0 GFLOPS on a 6144×6144 problem. (DJ: LINPACK; benchmarking; CRI CRAY Y-MP C90; NEC SX-3; MSC)

347 : Gordon Bell Prize for absolute performance awarded to Warren and Salmon, who achieves 5 GFLOPS on the Intel Touchstone Delta in a gravitational interaction tree code; prize for speedup awarded to Jones and Plassmann, who also achieves 5 GFLOPS on the same platform. Prize for price/performance awarded to Nakanishi, Rego, and Sunderam, whose Eclipse system achieves 1 GIPS per million dollars on a widely distributed network of workstations. (WGV: Gordon Bell Prize; distributed computing)

348 : The High Performance FORTRAN Forum (HPFF) is formed to define data-parallel extensions to FORTRAN. (MLF, ZH: HPF)

349 : MasPar starts delivering its second generation machine, the MP-2. Each machine contains up to 16K custom 32-bit processors, and is binary-compatible with the earlier MP-1. (WM: Maspar MP-2)

350 : Wavetracer closes doors. (MLF: Wavetracer)

351 : Anant Agarwal and others at MIT, LSI Logic, and Sun demonstrate the Sparcle, a modified SPARC which implements rapid context switching and supports user-level message-passing. The processor is used as a component in MIT's Alewife multiprocessor. (AA: Sparcle; MIT; LSI; Sun; Alewife; Agarwal, Anant)

352 : Kendall Square Research announces its KSR-1 after testing a system with 128 processors and a second level ring interconnect. (WM: KSR KSR-1)

353 : nCUBE introduces the nCUBE/2S family of systems based on yet another custom VLSI processor. (KV, BJ: nCUBE nCUBE/2S)

1993

354 : Version 1.0 of the High Performance FORTRAN (HPF) language specification is released. (MLF: HPF)

355 : Cray Research delivers a Y-MP M90 with 32 Gbyte of memory to the U.S. Government, after delivering a similar machine with 8 Gbyte of memory in the pre-

vious year to the Minnesota Supercomputer Center. (SD: CRI CRAY Y-MP M90)

356 : Fujitsu installs a one-of-a-kind 140-processor Numerical Wind Tunnel (NWT) machine at Japan's National Aerospace Laboratory (NAL). Each processor is a vector supercomputer with 256 Mbyte memory and a peak performance of 1.6 GFLOPS; processors are connected by crossbar network, and deliver aggregate LINPACK performance of 124.5 GFLOPS on 31920×31920 matrix. The technology in this machine is also used in Fujitsu's VPP-500 product. (HN, OY, LH, CC: Fujitsu VPP-500; NAL)

357 : IBM delivers the first SP1 Powerparallel system based on its RISC RS/6000 processor. (KHG, PS: IBM RS/6000)

358 : Silicon Graphics ships Challenge series of bus-based multiprocessor graphics workstations and servers, containing up to 36 MIPS R4400 RISC microprocessors. (SDE: SGI Challenge)

359 : Lawrence Livermore National Laboratory purchases a CS-2 Computing Surface from Meiko, the first major purchase by a U.S. national laboratory from a vendor with roots outside the U.S. (WGV: LLNL; Meiko CS-2)

360 : 512-node J-Machines (message-driven multicomputers) operational at MIT, Caltech, and Argonne National Laboratories. (DW: J-Machine; MIT; Caltech; ANL; Actors; Dally, Bill)

361 : IBM's GF-11 system (the name stands for 11 GFLOPS), purpose-built for quantum chromodynamic calculations under the direction of Monty Denneau, finishes computation of nucleon masses. (KHG: IBM GF-11)

362 : An NEC SX-3/44 with 4 processors achieves 15.1 GFLOPS (against a peak of 25.0) on 1000×1000 LINPACK; a Thinking Machines Corporation CM-5 achieves 59.7 GFLOPS with 1024 processors on a 52224×52224 problem. (DJ: LINPACK; benchmarking; NEC SX-3; TMC CM-5)

363 : Cray Computer Corp. places a CRAY-3 at the National Center for Atmospheric Research (NCAR). (BEA: CCC CRAY-3; NCAR)

364 : NEC produces the Cenju-3, containing up to 256 VR4400SC (MIPS R4000 runalike) processors connected by an Omega network. (TPD: NEC CENJU-3; Omega network)

365 : Sun begins shipping SPARCcenter 1000 and 2000 servers, shared-memory multiprocessor containing up to 8 and 20 SPARC CPUs respectively. (DPC: Sun; multiprocessor)

366 : ScaLAPACK prototypes released for Intel's Paragon, Thinking Machines' CM-5, and PVM message-passing system. (DJ: ScaLAPACK; PVM)

367 : CRI delivers first its first T3D multicomputer to the Pittsburgh Supercomputer Center. The machine contains a 3-dimensional torus of DEC Alpha microprocessors, and is hosted by a Y-MP C90. (WGV, PSC: CRI; CRI T3D; DEC Alpha)

3 Keywords

- ACPMAPS: 323
- ACS: 19